AN ULTRA WIDE BANDWIDTH POWER DIVIDER ON MMIC OPERATING 4 TO 10 GHZ

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ABSTRACT

A circuit topology has been developed to realize power dividers with bandwidths of 2.5:1 or greater on MMIC. A three-way divider has been fabricated which achieved 5.8 dB nominal insertion loss and 18 dB isolation from 4 to 10 GHz. This topology consists of lumped element interconnected networks and is thus ideally suited for MMIC technology.

I INTRODUCTION

Conventional power divider circuits operating at microwave frequencies utilize several quarter wavelength sections of transmission line to achieve multi-octave bandwidth performance. Such large structures are not realizable in monolithic microwave integrated circuit (MMIC) form, except perhaps for those which operate in Ku band or higher. While replacing the transmission lines with equivalent lumped element networks is possible, the resultant losses caused by several low Q MMIC components may be prohibitive. To realize power dividers on MMIC, a topology based on implementing the impedance transformation network with a minimum number of lumped elements is proposed. This topology is inherently low loss (minimum element) and has the potential to achieve wide bandwidths. Further, circuit component values are well suited for MMIC implementation in the 1 to 20 GHz region. Measured results from fabricated MMIC power divider circuits have demonstrated 2.5:1 bandwidths and 1 dB (from ideal) insertion losses.

The monolithic implementation overcomes many limitations in constructing planar three-way (or greater) circuits. Since the MMIC components are small, air bridge structures allow connecting isolation resistors between nonadjacent ports resulting in a nearly symmetric topology. Measured results from a three-way MMIC divider have demonstrated isolations greater than 20 dB.

II CIRCUIT DESCRIPTION

The circuit topology of the proposed N-way two-section power divider is depicted in Figure 1 for a divider with equal power division. The circuit consists of a series of N-arms to which circuitry is connected in either Y or delta configuration. The operation of this circuit is easily described using the concept of even and odd mode circuit analysis. Circuit symmetry allows decomposition into the even and odd mode circuits by applying proper voltage excitations at the output ports [1]. The

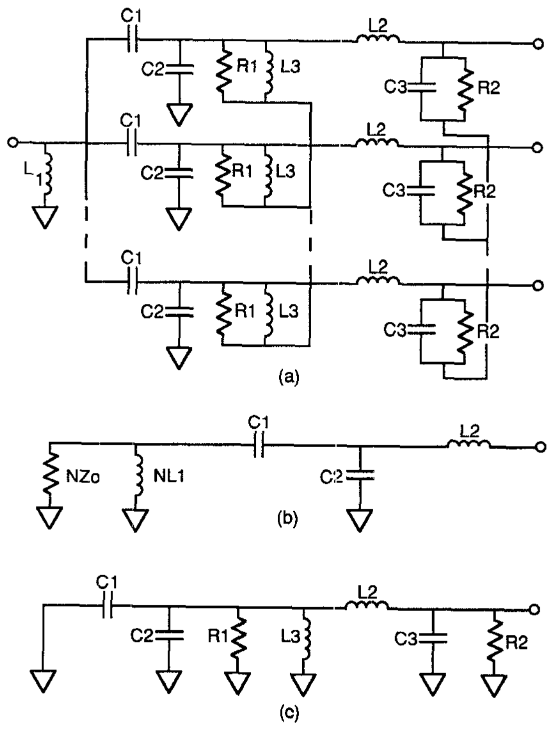

Figure 1 Wide bandwidth high performance power dividers have been implemented on MMIC using interconnected lumped element networks. a) MMIC power divider circuit topology. b) Equivalent even mode circuit. c) Equivalent odd mode circuit.

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resultant even and odd mode circuits are depicted in Fig. 1.

From the even and odd mode circuits, Scattering parameters for the power divider are [2, 3]:

$$S = \begin{bmatrix} A & T & T & T & . & . & T \\ T & B & C & . & . & . & C \\ T & C & B & C & . & . & C \\ . & . & . & . & . & . & . \\ . & . & . & . & . & . & C \\ T & C & C & C & C & B & C \\ T & C & C & C & C & C & B \end{bmatrix} \quad (1)$$

and

$$A = S^{+}_{11}$$
$$B = .5(S^{+}_{11} + S^{-}_{11})$$
$$C = .5(S^{+}_{11} - S^{-}_{11})$$
$$T = S^{+}_{11}/SQR(N)$$

where

S^{+}_{11} is the reflection coefficient of the even mode circuit

S^{-}_{11} is the reflection coefficient of the odd mode circuit

N is the number of outputs

Similar to distributed designs which utilize transmission lines, the function of the even mode circuit is to provide an impedance transformation between Zo and Zo*N ohms (Fig. 1). The transfer characteristics of this circuit (Eq. 1) dictate that of the divider, including bandwidth and insertion loss. Any deviation from the divider's ideal insertion characteristics are attributable to lossy components in the even mode circuit. Thus, for MMIC applications, the topology of this transformer is of paramount importance since it's realization is with low Q lumped elements. Hence, a minimum element topology with a Chebychev response is especially attractive for achieving wide bandwidth low loss performance. Further, as will be shown later, component values for a minimum element topology are well suited for implementation on MMIC.

The odd mode circuit (Fig. 1) also presents an impedance matching requirement. In this case, the input is short circuited, and the network must provide a resistive termination. In principle, a Chebychev response is also desirable. However, the short circuit condition (at the input) removes L1 from the odd mode circuit. The result is an odd mode circuit of lower order than the even mode one. To alleviate this condition, inductor L3 and capacitor C3 are included with the isolation resistors. This allows approximating an odd mode Chebychev response by selecting proper values for R1, R2, C3, and L3.

III ANALYTICAL DESIGN TECHNIQUES

Design equations for the even mode circuit components are based on filter design concepts [4-6]. To achieve a minimum element network with a Chebychev response, the ripple factor of the low pass prototype is adjusted to maximize the transformation ratio (N_{max}) per a constrained bandwidth. This condition is defined as:

$$Q_T = \frac{f_1 \, f_2}{f_2 - f_1} \quad (2)$$

then

$$N_{max} = 1 + Q_T^2 g_i g_{i+1} \quad (3)$$

where

g_i are the low pass prototype elements, and

f_1, f_2 are the band edge frequencies.

The low pass prototype is now transformed and reduced to a minimum element bandpass structure (Fig. 2). Higher order topologies can be developed as cascades of these networks or sub-networks. Since the network transformation results in two circuits, an alternative power divider topology is obtained by interchanging inductors and capacitors in Fig. 1. However, for MMIC realization, component values for the prior topology (Fig. 2b) are more realizable than the latter.

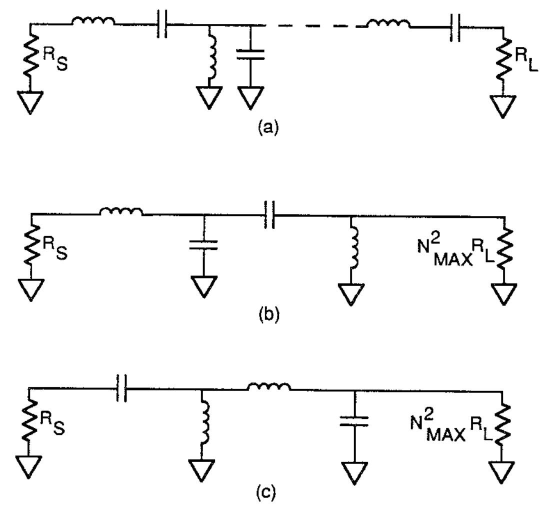


Figure 2 The impedance transformer is implemented as a minimum element bandpass circuit. a) General low pass prototype b) c) Band pass circuit topologies (n=2).

A further requirement of the impedance transformation (even mode) circuit is wide bandwidth low loss performance. To this end, a network composed of a minimum number of elements and with realizable values is desirable. Bandwidth performance, which is dependent on the minimum allowable return loss and impedance transformation ratio (N) is depicted in Fig. 3 for the minimum element network. The ability to realize these values on MMIC can be seen in the design of a three-way divider operating from 4 to 10 GHz. For this design, (Fig. 1a) the component values tabulated in Table I are easily realizable in monolithic form as MIM capacitors and air bridge inductors.

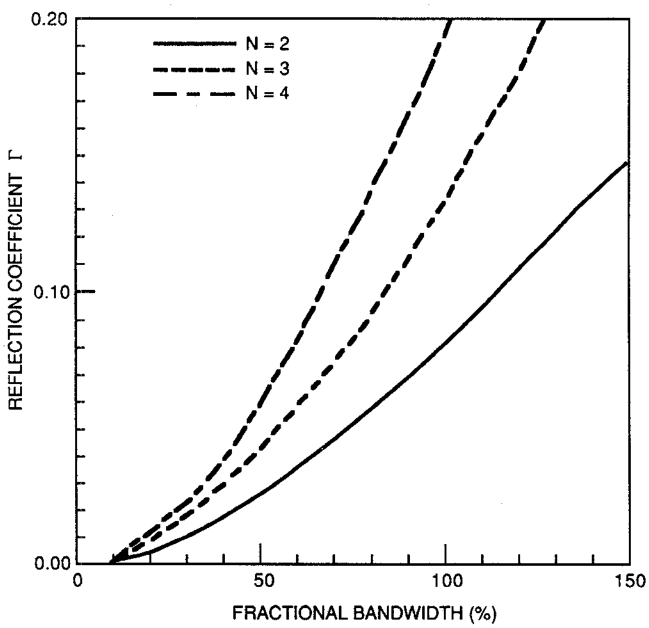


Figure 3 Reflection coefficient and bandwidth relationship of minimum element impedance transformers. Parameter N is the transformation ratio.

TABLE I

Component values for a three-way divider operating 4 to 10 GHz

Component	value
L_1	1.53 nH
C_1	0.404 pF
C_2	0.209 pF
L_2	1.03 nH

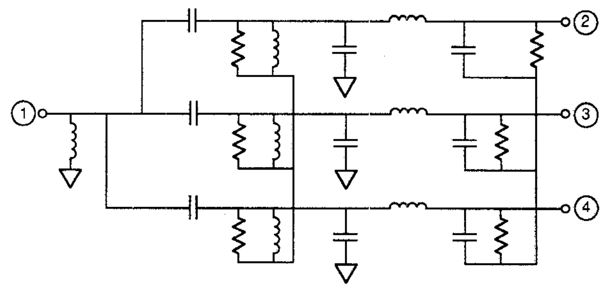
Design equations for the odd mode circuit are based on approximating a Chebychev response. A convenient method of approximating this condition is by equating zeros of the odd and even mode circuits [7]. Since, the odd mode circuit reflection coefficient is given as:

$$\Gamma_o = \frac{(S - S_{a1})\ (S - S_{a2})\ \ . \ . \ .}{(S - S_{b1})\ (S - S_{b2})\ \ . \ . \ .} \qquad (4)$$

each zero should in principle be equated to the even mode ones. Thus, values for components R1, R2, L3, and C3 are obtained. All other component values are constrained by the even mode circuit.

IV MEASURED PERFORMANCE

Using the previously mentioned concepts, a three way passive power divider operating from 4 to 10 GHz was designed on MMIC based on the topology of Figure 1.0. For this design, a minimum element topology was derived for a fractional bandwidth of 95%. This fractional bandwidth defined the even mode circuit, and also the input of the



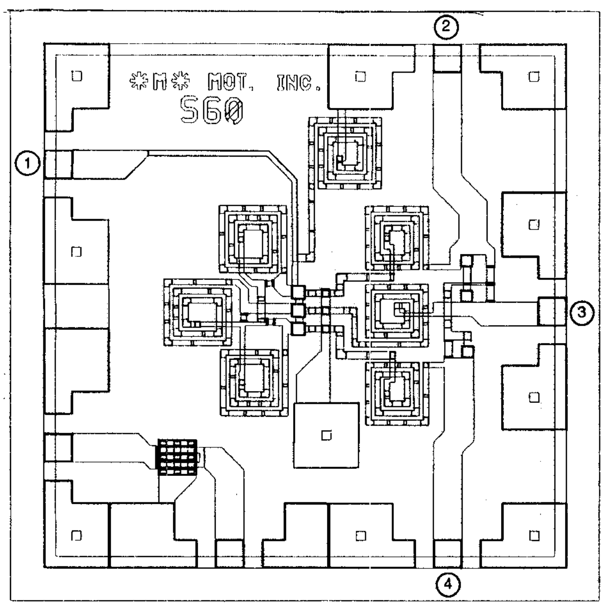


Figure 4 Schematic and layout of a three way MMIC power divider operating from 4 to 10 GHz. All circuitry is easily accommodated on a 60 x 60 mil chip.

power divider, to 17.5 dB return loss (Figure 3.0). Component values for the odd mode circuit were derived by equating zeros of the two circuits.

The circuit was designed on a 60x60 mil chip and included RF probe pads at each port to allow measuring on-chip performance (Fig. 4). All circuit components were realized as MIM capacitors, NiCr resistors, and air bridge inductors. A short length of high impedance transmission line was included at the input of the divider to compensate for the parasitic nature of the lumped elements.

Excellent agreement was obtained between

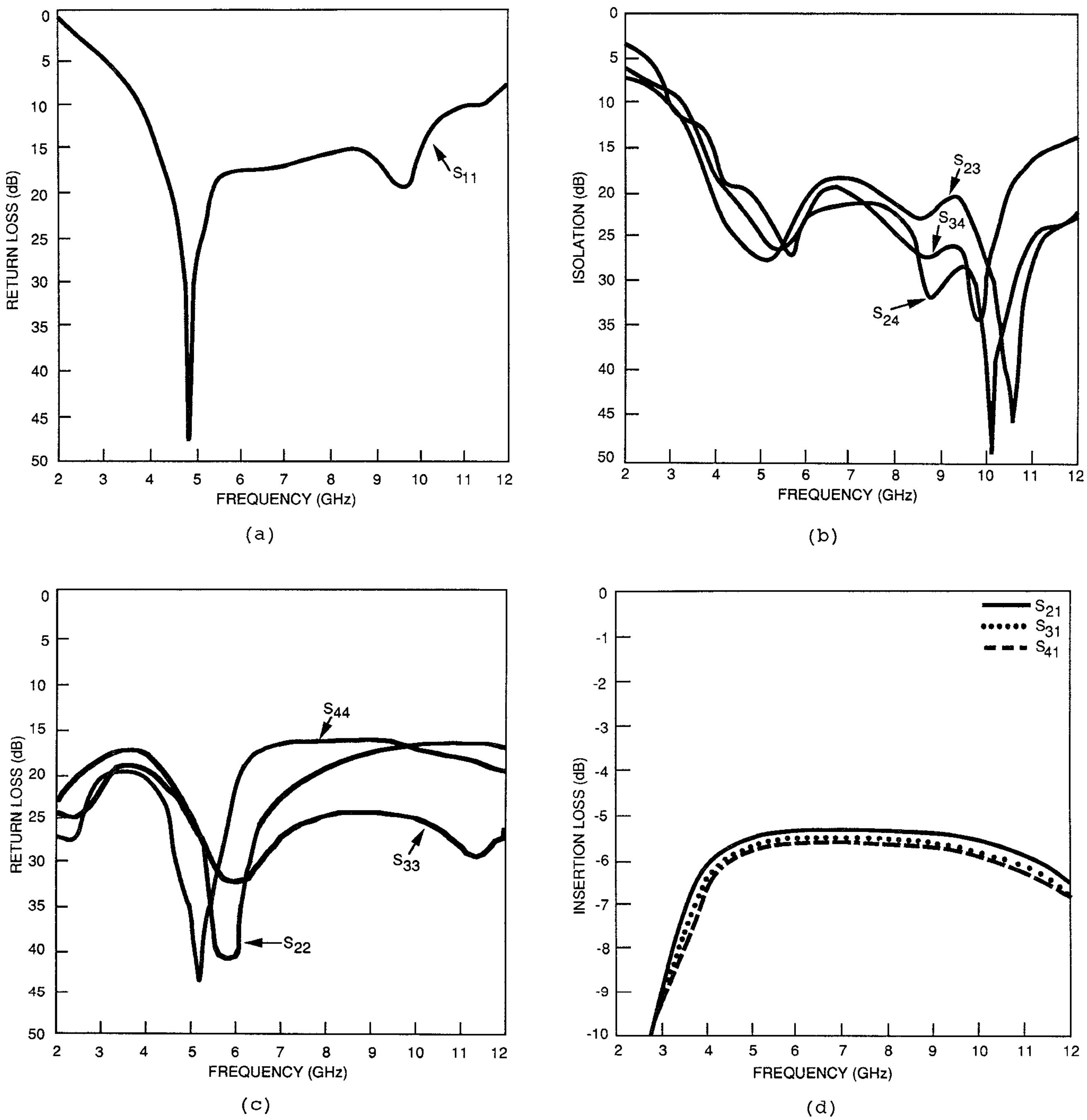


Figure 5 Measured performance from a three way power divider has demonstrated 2.5:1 or greater bandwidths are realizable on MMIC using lumped topologies. a) Input return loss. b) Output to output isolation. c) Output return loss. d) Insertion characteristics.

measured and predicted performance. Over the operational bandwidth of 4 to 10 GHz, the measured insertion loss was generally 5.8 dB (4.8 dB is ideal) with the loss at the band edges being slighly higher (Figure 5). This higher loss is due to the low component Q. Insertion loss between each output port are nearly similar and track within .5 dB of each other. The input/output return losses are generally better than 15 dB. Further, this value (15 dB) compares closely to the 17.5 dB value for a lossless topology. Excellent output to output isolation (which is greater than 20 dB) reflects a well matched odd mode and the high symmetry provided by the air bridge connections of the odd mode circuitry to each of the three main arms.

V SUMMARY

Circuit simulations and measured performance from fabricated MMIC circuits have demonstrated that wide bandwidth low loss passive powers can be implemented on MMIC. The proposed minimum element topology favors component values which are easily realizable and thus minimize losses due to low Q elements. Measured performance of a 3 way divider operating between 4 to 10 GHz on MMIC is very encouraging. These results are comparable to those obtained with microstrip distributed designs using transmission lines!

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